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6. AUTHOR(S)
Dr. James Van Hove

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
SVT Associates, Inc.
7620 Executive Drive
Eden Prairie, MN 55344

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Office of Naval Research
ONR 254 Russelle Dunson
Ballston Tower One
800 North Quincy Street
Arlington, VA 22217-5660

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This report summarizes the first month on the SBIR Phase I program to develop AlGaN Channel JFETs. A mask set to fabricate nitride based JFETs was begun. IV curves of GaN PN junctions are shown. Measurements of the leakage of these junctions indicate that recessing the P layer routinely will require an etch stop to minimize the leakage current. Ni Au P type ohmics did not withstand 500 C anneals.

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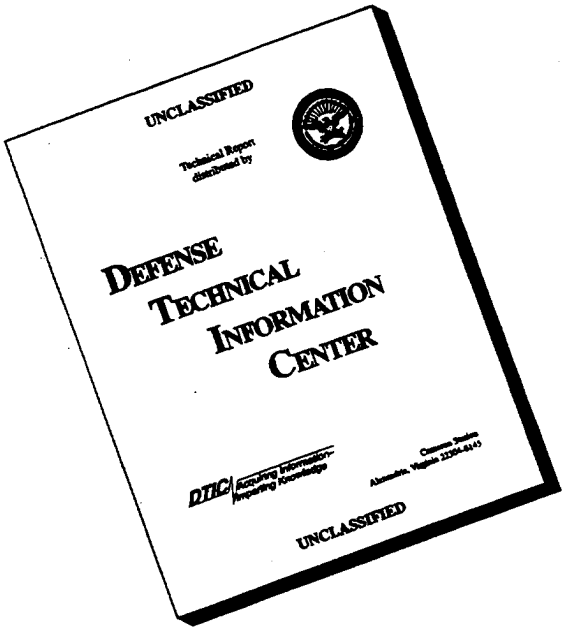

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AlGaN Channel Transistors for Power Management and Distribution.

Progress Report 1
Phase I SBIR Contract N00014-96-C-0251
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Submitted to:

Dr. Colin Wood, Code 312
Program Officer
Office of Naval Research
800 North Quincy Street
Arlington, Virginia 22217-5660

Submitted by:

Dr. James M. Van Hove
SVT Associates
7620 Executive Drive
Eden Prairie, MN 55344
(612) 934-2100 ext. 225
(612) 934-2737 Fax
jvanhove@svta.com

AlGaN Channel Transistors for Power Management and Distribution.

Summary
This report summarizes the first month on the SBIR Phase I program to develop AlGaN Channel JFETs. A mask set to fabricate nitride based JFETs was begun. IV curves of GaN PN junctions are shown. Measurements of the leakage of these junctions indicate that recessing the P layer routinely will require an etch stop to minimize the leakage current. Ni Au P type ohmics did not withstand 500 °C anneals.

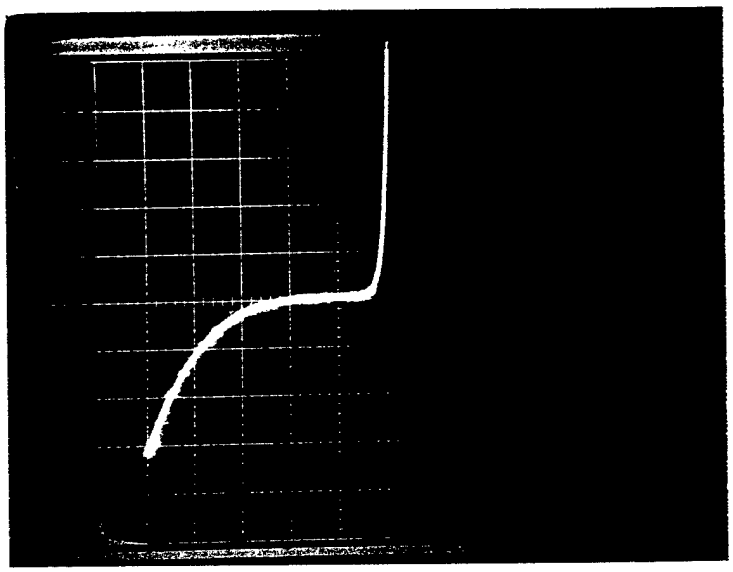
Progress Report
During the first month of this program, we began by designing a mask to fabricate the JFET devices. This is still not completed and will be finished by the end of month two. The MBE system went down during the second week of May due to a power failure which resulted in both an Al and Ga crucible failure. The Mg ion source discussed in the proposal was added during the repair. The system is being outgassed and dopant sources characterized at this time. A GaN PN junction was deposited on sapphire prior to the MBE system going down. This structure was fabricated into large area (300 x 300 μm) junctions using a mask set used to make UV detector arrays. The structure consisted of 3000 Ä of P type GaN doped about $2x10^{17}$ cm^{-3} on top of 4000 Ä of $5x10^{16}$ cm^{-3} N type GaN. This structure was used for UV detectors and is not optimized for the JFET. The P type material was recessed using a $SiCl_4$ based RIE to remove just the top 3000 Ä of material.. This step is critical for the JFET fabrication since the P type region must be removed everywhere except under the gate region. Overetching of the P layer into the N layer will result in reduced current through the JFET. Any P type material which remains, however, will reduce the breakdown voltages and increase the leakage currents. Contacts were made to both the N and P type regions. Figure 1 shows the current-voltage curves for two different devices located in the center and edge of the two inch sapphire wafer. The leakage current increased from the center to the edge. This corresponded to the non-uniformity of the RIE process over the two inch wafer. The edges were not recessed as deeply as expected.

The non-uniformity of the leakage current across the wafer indicates that a etch stop will have to be used to recess the gate P type layer. The measured leakage did not increase with area but is still much higher than expected. This may be the result of P type material still remaining even in the center of the wafer. RIE is known to cause damage to III-V materials and this may be causing increased leakage although no area or circumference relationship was noted. Ni Au was used for the P type ohmics. They did not survive a 500 °C anneal and will have to be changed to a refractory metal such as W for the gate electrode.

Future Plans

During the next two months, the mask set will be finished and the JFET layer structures designed. The JFET structure will be grown but probably not processed due to the time required to obtain the mask set. Measurements of the leakage and breakdown characteristics will be made with the existing detector mask set.

a)



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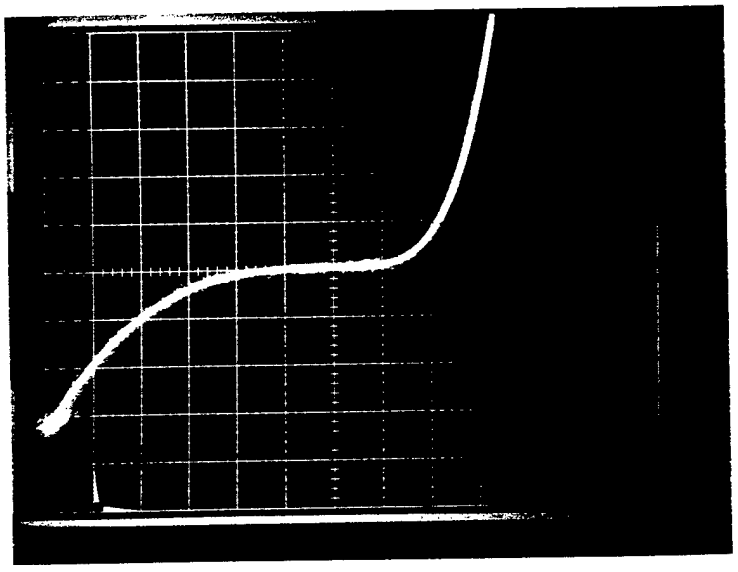

Figure 1. Current voltage curves for GaN PN junctions (350 μm octagons). a) Curve taken from the center of the wafer. The scales are 2V/ div. hor. and 50 μa/div vert., b) Curve from edge of wafer. The scales are 0.5 V/div. hor. and 50 μa/div vert.